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09/727,297	11/29/2000	Francesco Pappalardo	854063.596	4071

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EXAMINER	
BELL, MELTIN	

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2121	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/727,297	Applicant(s) PAPPALARDO ET AL.	
	Examiner Meltin Bell	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/29/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/3-9-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to application **09/727,297** filed 11/29/00 as well as the IDS, priority documents and solicitation for reconsideration filed 3/9/04. Currently amended and original claims 1-17 filed by the applicant have been entered and examined. As presented later in this Office Action, the currently amended and original claims 1-17 are not persuasive for being anticipated by prior art. The status of the application since the last action was mailed 10/9/03 follows.

Priority

Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Acknowledgment is made of applicant's claim for foreign priority based on application T099A 001056 filed in Italy on **11/30/99**. The certified copy of the T099A 001056 application was received with the 3/9/04 Information Disclosure Statement.

Information Disclosure Statement

The 3/9/04 IDS listing the Watanabe et al reference's month of publication missing in the 11/29/00 IDS is noted.

RESPONSE TO APPLICANTS' ARGUMENTS

Drawings

Applicant(s) argue(s) that "The drawing was objected to because it was not labeled "Figure 1." The applicants respectfully traverse this objection because the Rules require the drawing to not be labeled. Specifically, 37 CFR § 1.84(u)(1) states, "Where only a single view is used in an application to illustrate the claimed invention, it must not be numbered and the abbreviation "FIG." must not appear" (REMARKS page 7, paragraph 2). Accordingly, the original drawing is correct as filed." The objection to the drawing is withdrawn.

Specification

Applicant(s) argue(s) that "The specification was objected to because the examiner asserted that Figure 1 should be listed in the Brief Description of the Drawings section. As discussed above, the single drawing provided with the application cannot be labeled "Figure 1" according to Rule 84(u)(1). As a result, "Figure 1" is correctly not listed in the Brief Description of the Drawings section" (REMARKS page 7, paragraph 3). This objection to the specification is withdrawn. However, the specification is further objected to for the "fourth output datum" typo of claim 2 on page 2, line 17 of the specification.

Claim Rejections - 35 USC § 112, first paragraph and 35 USC § 101

Applicant(s) argue(s) that "Claim 12 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Further, claim 12 was rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Specifically, the Examiner noted that claim 12 was not claimed to be practiced on a computer. Claim 12 is being amended to recite that the invention is practiced on a computer as suggested by the Examiner. Such an amendment highlights the practical utility of the claimed method which performs logical fuzzy union and intersection operations. Moreover, the specification describes in detail how to make and user the invention recited in amended claim 12. Accordingly, amended claim 12 is properly enabled within the meaning of Section 112, first paragraph, and is supported by a well-established utility within the meaning of Section 101" (REMARKS page 7, paragraphs 4-5). The 35 U.S.C. § 112, first paragraph and 35 U.S.C. § 101 rejections of claim 12 are withdrawn.

Claim Rejections - 35 USC § 112, second paragraph

Applicant(s) argue(s) that "Claims 2 and 10 were rejected under 35 U.S.C. § 112, second paragraph , as being indefinite. Claims 2 and 10 are being amended to provide proper antecedent bases for the limitations noted by the Examiner. Therefore, amended claims 2 and 10 particularly point out and distinctly claim the invention" (REMARKS page 7, paragraph 6). The 35 U.S.C. § 112, second paragraph rejections of claims 2 and 10 are withdrawn.

Claim Rejections - 35 USC § 102 and 35 USC § 103

Applicant(s) argue(s) that "Claims 1 and 4-17 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,343,553 to Miyazawa et al. ("Miyazawa")" (REMARKS page 7, paragraph 7), "Miyazawa does not disclose the invention recited in claims 1 and 4-17" (REMARKS page 7, paragraph 8, sentence 1), "Miyazawa does not disclose the comparator means as recited in claim 1. The Examiner correctly notes that Miyazawa refers to a calculation unit with a multiplier or divider for multiplying or dividing a difference by a one of values which is in accordance with a plus or minus sign of the difference. Miyazawa does not suggest that the multiplying or dividing involves any comparison, and especially not a comparison of a sign flag and a first selection signal for selecting a logical fuzzy union operation or a logical fuzzy intersection operation. Moreover, the Miyazawa multiplier or divider receives at input a difference and a value in accordance with a plus or minus sign, and nothing in Miyazawa suggests that the difference is a first selection signal for selecting a logical fuzzy union operation or a logical fuzzy intersection operation" (REMARKS page 8, paragraph 2), "Miyazawa also does not disclose the first selection means as recited in claim 1. The Examiner notes that Miyazawa shows a data selection means in Figure 31, but nothing in Figure 31 or the accompanying text suggest a data selection means that is connected as recited in claim 1 or that performs the function of the first data selection means recited in claim 1" (REMARKS page 8, paragraph 3, sentences 1-2), in Miyazawa "The selector 391 receives the same inputs XL, XR, XO, as the subtracter 392, but does not have a

selection input connected to the output of any comparison means that it connected to the output of the subtracter 392. The only element connected to the output of the subtracter 392 is the multiplier 395, but the output of the multiplier 395 is not connected to a selection input of the selector 391" (REMARKS page 8, paragraph 3, sentences 4-5), "For the foregoing reasons, claim 1 is not anticipated by Miyazawa" (REMARKS page 9, paragraph 2), "Claims 4-7 depend on claim 1, and thus, are not anticipated by Miyazawa for the reasons expressed above. In addition, claim 4 further recites that the comparison means comprise identity detection means that are not disclosed by Miyazawa. The Examiner points to Figure 36 of Miyazawa as showing identify selection means but nothing in Figure 36 or the accompanying text suggests that any part of Figure 36 implements an identify function in which a second selection signal assumes a first level when a sign flag and a first selection signal are identical to each other and a second level when the sign flag and the first selection signal are different from each other. Assuming that the Examiner is suggesting that the inputs CB and FT are the sign flag and first selection signal of claim 4, the circuit 403 produces a first output o1 that is zero when FT is zero and equal to oS when FT is one, regardless of the value of CB. As such, the first output o1 cannot be the second selection signal generated by an identify detection means as recited in claim 1" (REMARKS page 9, paragraph 3), "For the foregoing reasons, claims 4-6 are not anticipated by Miyazawa" (REMARKS page 9, paragraph 5), "Miyazawa does not disclose the invention recited in claims 8-11...Although the Examiner has pointed to elements of Miyazawa that are said to be the subtacter and multiplexers recited in claim 8, the elements pointed to by the

Examiner are not connected as recited in claim 8. For example, claim 8 recites that the first multiplexer has first and second data inputs that receive the same first and second input data that are received by the first and second inputs of the subtracter. The Examiner points to the coefficient setters 396, 397 as the multiplexers, but neither coefficient setter has inputs connected to the same input data" (REMARKS page 9, paragraph 6), "that are received by the first and second inputs of either of the subtracters 390, 392...Neither of the coefficient setters 396, 397 has an input coupled to the output of the other coefficient setter" (REMARKS page 10, paragraph 1), "For the foregoing reasons, claim 8 is not anticipated by Miyazawa" (REMARKS page 10, paragraph 3), and "Claims 9-11 depend on claim 8, and thus, are also not anticipated by Miyazawa. In addition, claims 9-11 recite additional language that, while not identical to that of claims 1, 4, and 6, further distinguish claims 9-11 from Miyazawa for reasons similar to those expressed above for claims 1, 4, and 6" (REMARKS page 10, paragraph 4).

Applicant(s) argue(s) that "Claims 2 and 3 were rejected under 35 U.S.C. § 103 as being unpatentable over Miyazawa in view of U.S. Patent No. 5,335,314 to Tsutsumi et al. ("Tsutsumi"). Miyazawa and Tsutsumi do not teach or suggest the invention recited in claims 2-3. Claim 2 depends on claim 1, and thus, includes the comparator means and first selector means that are not taught by Miyazawa as discussed above with respect to claim 1. Tsutsumi likewise does not teach or suggest the comparator means and first selector means, and the Examiner does not claim that it does. For those

reasons alone, claims 2-3 are nonobvious in view of Miyazawa and Tsutsumi" (REMARKS page 10, paragraphs 6-7)", "Similar to the discussion above with respect to claim 8, neither the selectors 391, 401 nor the coefficient setters 396, 397 have inputs connected to the output of a subtracter or the output of a first data selection means" (REMARKS page 11, paragraph 1, sentence 2), "Claim 2 also recites...The Examiner admits that Miyazawa does not teach such features, but asserts that Tsutsumi supplies the missing teaching in Figs 1, 4, 11, 14, and 15 and the Abstract. However, those figures of Tsutsumi clearly show both a fuzzy output and a non-fuzzy output being provided at separate outputs of the concluder section 110 without selecting either a fuzzy output or a non-fuzzy output based on a selection signal. Thus, Tsutsumi does not teach or suggest any of the features of claim 2 that are missing from Miyazawa" (REMARKS page 11, paragraph 2) and "For the foregoing reasons, claims 2-3 are nonobvious in view of Miyazawa and Tsutsumi" (REMARKS page 12, paragraph 3).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Office presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Office to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Original and currently amended claims 1-2, 4, 8 and 12 stand rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over *Miyazawa et al* USPN 5,343,553 (August 30, 1994).

Regarding claim 1:

Miyazawa et al teaches,

- subtracter means having a first and a second input receiving a first and, respectively, a second input datum; a first output supplying a first output datum correlated to the difference between said first and second input datum; and a second output supplying a sign flag indicating the sign of said first output datum (Fig. 31, item 390; column 14,

lines 48-68, "a first subtracter...subtracter 390 and"; column 15, lines 1-2, "form parameters K0...coefficients k1 to k4")

- comparison means having a first input receiving said sign flag, a second input receiving a first selection signal assuming a first level for the selection of said logical fuzzy union operation and a second level for the selection of said logical fuzzy intersection operation; and an output supplying a second selection signal assuming a first level when said sign flag and said first selection signal comply with a pre-determined relation and a second level when said sign flag and said first selection signal do not comply with said pre-determined relation (Fig. 31, item 394; Figs. 50, 65; column 17, lines 9-13, "The minimum-value calculation in...the maximum value"; column 17, lines 25-50, "In FIG. 49 is illustrated...binary code B"; column 23, lines 56-63, "maximum-value calculation...a digital comparator"; column 24, lines 4-46, "an example of...maximum-value calculation circuit")

- first data selection means (Fig. 31, item 391)

However, *Miyazawa et al* doesn't explicitly teach first data selection means having a first and a second datum input receiving said first and, respectively, said second input datum; a selection input connected to said output of said comparison means and receiving said second selection signal; and an output supplying a second output datum correlated to one of said first and second input data as a function of the level of said second selection signal. Although the structure of the fuzzy inference circuits differ, it would have been obvious to one of ordinary skill in the art at the time the invention was

made for simplifying construction of a fuzzy circuit (*Miyazawa et al*, column 2, lines 10-14, "It is another...simple in construction").

Regarding claim 2:

The rejection of claim 1 is incorporated. Claim 2's further limitations are taught in *Miyazawa et al*:

- second data selection means having a first and a second datum input connected to said output of said first data selection means and, respectively, to said first output of said subtracter means and receiving said first and, respectively, said second output datum; a selection input receiving a third selection signal assuming a first level for the selection of an operating mode in fuzzy logic and a second level for the selection of an operating mode in non-fuzzy logic; and an output supplying a third output datum correlated to one of said first and second output datum as a function of the level of said third selection signal (Abstract, "A digital fuzzy...one definite value"; Fig. 31, items 396, 397; column 15, lines 7-19, "First and second...in equations (7) to (10)"; column 23, lines 5-15, "FIG. 62 is a block...the data selectors 133a, 132b"; Fig. 76, items 280-285; column 28, lines 39-62, "The above subtractions...multiplexers 283 to 285")

Therefore, claim 2 is rejected under the same rationale as claim 1.

Regarding claim 4:

The rejection of claim 1 is incorporated. Claim 4's further limitations are taught in *Miyazawa et al*:

- said comparison means comprise identity detection means generating said second selection signal assuming said first level when said sign flag and said first selection

signal are identical to each other and said second level when said sign flag and said first selection signal are different from each other (Fig. 36, item 403, chip QC5, outputs oG, oE, oS; column 16, lines 8-12, "FIG. 36 shows slope coefficient...between conditions of Xi<XL and xo ≧ xi ≧ xL")

Therefore, claim 4 is rejected under the same rationale as claim 1.

Regarding claim 8:

Miyazawa et al teaches,

- a subtracter having first and second inputs that receive first and second input data, respectively, and first and second outputs, the subtracter being structured to produce at the first output a first output datum equal to the difference between the first and second input data; and produce at the second output a sign flag indicating whether the difference is positive or negative (Fig. 31, item 390; column 14, lines 48-68, "a first subtracter...subtracter 390 and"; column 15, lines 1-2, "form parameters K0...coefficients k1 to k4")

- first and second multiplexers (Fig. 31, items 391, 396, 397; column 15, lines 7-19, "First and second...in equations (7) to (10)"; column 23, lines 5-15, "FIG. 62 is a block...the data selectors 133a, 132b"; Fig. 76, items 280-285; column 28, lines 39-62, "The above subtractions...multiplexers 283 to 285")

However, *Miyazawa et al* doesn't explicitly teach a first multiplexer having first and second data inputs, a control input, and an output, the first and second data inputs receiving the first and second input data, respectively; the control input being coupled to the second output of the subtracter, and the first multiplexer being structured to supply

at the output of the first multiplexer a one of the first and second input data which is selected depending on the sign flag or a second multiplexer having a first and a second data inputs, a control input, and an output, the first and second data inputs being coupled to the first output of the subtracter and the output of the first multiplexer, respectively. Although the structure of the fuzzy inference circuits differ, it would have been obvious to one of ordinary skill in the art at the time the invention was made for simplifying construction of a fuzzy circuit (*Miyazawa et al*, column 2, lines 10-14, "It is another...simple in construction"). Although the structure of the fuzzy inference circuits differ, it would have been obvious to one of ordinary skill in the art at the time the invention was made for simplifying construction of a fuzzy circuit (*Miyazawa et al*, column 2, lines 10-14, "It is another...simple in construction").

Regarding claim 12:

Miyazawa et al teaches,

- determining a difference between the first and second inputs, resulting in a difference value corresponding to the difference and a sign flag indicating a sign of the difference (Fig. 31, item 390; column 14, lines 48-68, "a first subtracter...subtracter 390 and"; column 15, lines 1-2, "form parameters K0...coefficients k1 to k4")
- comparing the sign flag with a first selection signal having a first value if the fuzzy logical union operation is selected and a second value if the logical fuzzy intersection operation is selected, the comparing resulting in second selection signal having a first level when the sign flag and the first selection signal comply with a predetermined relation and a second level when the sign flag and the first selection signal do not

comply with the predetermined relation (Fig. 31, item 394; Figs. 50, 65; column 17, lines 9-13, "The minimum-value calculation in...the maximum value"; column 17, lines 25-50, "In FIG. 49 is illustrated...binary code B"; column 23, lines 56-63, "maximum-value calculation...a digital comparator"; column 24, lines 4-46, "an example of...maximum-value calculation circuit")

- data selection (Fig. 31, item 391)

However, *Miyazawa et al* doesn't explicitly teach selecting as a first output one of the first and second inputs depending on whether the second selection signal has the first level or the second level. Although the structure of the fuzzy inference circuits differ, it would have been obvious to one of ordinary skill in the art at the time the invention was made for simplifying construction of a fuzzy circuit (*Miyazawa et al*, column 2, lines 10-14, "It is another...simple in construction").

Original and currently amended claims 3, 5-7, 9-11, and 13-17 stand rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over *Miyazawa et al* USPN 5,343,553 (August 30, 1994) for being dependent on the above rejected independent claims and for reasons given in the prior office action.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- *Miyazawa et al*; U.S. Patent Number 5,343,553; Digital Fuzzy Inference System Using Logic Circuits
- *Tsutsumi et al*; U.S. Patent Number 5,335,314; Fuzzy Inference Apparatus
- *Pappalardo et al*; U.S. Patent Number 5,875,438; Method for storing membership functions and related circuit for calculating a grade of membership of antecedents of fuzzy rules
- *Giacalone et al*; U.S. Patent Number 6,385,598; Fuzzy processor with architecture for non-fuzzy processing
- *Giacalone et al;* U.S. Patent Number 5,710,867; Method for parallel processing of fuzzy logic inference rules and corresponding circuit architecture with fuzzy inputs and outputs

- *Abruzzese et al;* U.S. Patent Number 5,615,303; Circuit for computing membership function values in a fuzzy logic controller

- *Mazza et al;* U.S. Patent Number 6,075,338; Driving of a three-phase motor with fuzzy logic control of the slip

- *Pappalardo et al;* U.S. Patent Number 6,424,958; Coding and storing method for fuzzy logic rules and circuit architecture for processing such rules

- *Matranga et al;* U.S. Patent Number 5,796,917; Method and apparatus for parallel processing of fuzzy rules

- *Giacalone et al;* Hardware implementation versus software emulation of fuzzy algorithms in real applications; The IEEE International Conference on Fuzzy Systems Proceedings; Vol. 1; 4-9 May 1998; pp 7-12

- *Gabrielli et al;* Design and preliminary results of high speed analog 1.0 μm CMOS MIN-MAX circuit for fuzzy architectures; Proceedings of the 38th Midwest Symposium on Circuits and Systems; Vol. 1; 13-16 Aug. 1995; pp 381-384

- *Hung et al;* Implementing a fuzzy inference engine using FPGA; Sixth Annual IEEE International ASIC Conference and Exhibit Proceedings; 27 Sept.-1 Oct. 1993; pp 349-352

- *Kartika;* FPGA Application As Irrigation Controller With Fuzzy Logic Methode; www.tec.puv.fi/~smv/ED1/PROJECT/xs_fuzzy.pdf

Any inquiry concerning this communication or earlier communications from the Office should be directed to Meltin Bell whose telephone number is 703-305-0362. This Examiner can normally be reached on Mon - Fri 7:30 am - 4:30 pm.

If attempts to reach this Examiner by telephone are unsuccessful, his supervisor, Anil Khatri, can be reached on 703-305-0282. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MB

Anthony Knight
Supervisory Patent Examiner
Group 3600